sub. A7

add A9

Patent Claims

1. A circuit arrangement having a load transistor (T1) and a current sensing transistor (T2) coupled to the load transistor (T1),

characterized in that

a switch arrangement (SW) having at least one first switch (S1; S1a, S1b) is connected downstream of the current sensing transistor (T2) in order to connect the current sensing transistor (T2) to a first or second evaluation circuit (BL1, BL2) depending on a control signal (AS).

2. The circuit arrangement as claimed in claim 1, in which the switch (S1; S1a, S1b) is driven depending on a voltage (UDS) across the load path (D-S) of the load transistor (T1).

3. The circuit arrangement as claimed in claim 1 or 2, in which the switch arrangement (S) feeds an output current (I_s) of the current sensing transistor (T2) to a first or second processing unit (BL1, BL2).

4. The circuit arrangement as claimed in one of the preceding claims, in which the load transistor (T1) and the current sensing transistor (T2) are integrated in a first chip (IC1), and in which the switch arrangement (SW) and the first and

second evaluation circuits (BL1, BL2) are integrated in a second chip (IC2).

5. The circuit arrangement as claimed in one of the preceding claims, in which the switch arrangement (S) has a comparator arrangement (K1), which compares the load path voltage of the load transistor (T1) with a reference voltage (Uref).

6. The circuit arrangement as claimed in claim 5, in which the first switch (S1; S1a, S1b) is driven depending on an output signal (AS) of the comparator arrangement (K1).

7. The circuit arrangement as claimed in one of the preceding claims, in which the first switch (S1a, S1b) has a first and a second transistor (S1a, S1b), which are driven depending on the output signal of the comparator arrangement (K1).

8. The circuit arrangement as claimed in one of the preceding claims, in which the first evaluation circuit (BL1) has a second comparator arrangement (K2) and a resistor (T3), which can be regulated by means of the comparator arrangement (K2) and is connected in series with the current sensing transistor (T2).

9. The circuit arrangement as claimed in claim 8, in which the second processing unit (BL2) has a further resistor (R1)

in series with the regulatable resistor (T3), and a first current signal (Us1) can be tapped off at said further resistor.

10. The circuit arrangement as claimed in claim 8 or 9, in which the regulatable resistor (T3) is designed as a transistor.

11. The circuit arrangement as claimed in one of the preceding claims, in which the second processing unit (BL2) has a series circuit comprising a second resistor (R2) and a second switch (T4) in series with the current sensing transistor (T2).

12. The circuit arrangement as claimed in claim 10, in which the second switch (T4) is driven depending on a switch position of the switch arrangement (S2; S2a, S2b).

13. The circuit arrangement as claimed in one of the preceding claims, in which a load path of the first transistor (S1a) is connected up between a terminal for a supply potential (Vdd) and a control terminal of the regulatable resistor (T3).

14. The circuit arrangement as claimed in one of the preceding claims, in which a load path of the second

transistor (S1b) is connected up between a supply potential and a control terminal of the second switch (T4).